

NON-VOLATILE PRODUCT TERM (PTERM) CELL

ABSTRACT

A non-volatile product term cell is provided having a first floating gate located over a first p-channel transistor and a first n-channel transistor, and a second floating gate located over a second p-channel transistor and a second n-channel transistor. A control gate is located over the first and second floating gates. A first tunnel oxide capacitor is coupled to the first floating gate and a second tunnel oxide capacitor is coupled to the second floating gate. A first transistor pair is coupled between the first p-channel transistor and the second n-channel transistor, and a second transistor pair is coupled between the second p-channel transistor and the first n-channel transistor. The first and second floating gates are programmed and/or erased. Complementary input signals are applied to the first and second transistor pairs. An output signal is provided in response to the programmed/erased states of the first and second floating gates.